## IN THE CLAIMS

Please enter the following amendments to the claims. The amendments are believed to introduce no new matter.

1. (Currently Amended) A method for testing arbitration logic or bus-mastering logic associated with a digital logic device, the method comprising:

receiving a request at a secondary component coupled to a primary component through arbitration logic, the request characteristic of a primary component request;

determining a pseudo-random delay at the secondary component prior to responding to the request; and

sending a response from the secondary component after the pseudo-random delay, the response corresponding to the request.~~pseudo-randomly delaying a response to the request.~~

2. (Currently Amended) The method of claim 1, wherein the pseudo-random delay is used to adjust the wait-state of the secondary component, wherein the wait-state is an amount of time the primary component has to wait before the secondary component accepts the request.~~ pseudo-randomly delaying comprises: adjusting the wait-state and/or latency.~~

3. (Currently Amended) The method of claim ~~2~~1, wherein the pseudo-random delay is used to adjust the latency of the secondary component, wherein the latency is an amount of time the secondary component takes to satisfy the request.~~ adjusting the wait-state and/or latency comprises: selecting a time-delay from a delay mechanism.~~

4. (Currently Amended) The method of claim 3, wherein ~~the~~ a delay mechanism used to introduce the pseudo-random delay is a linear feedback shift register.

5. (Currently Amended) The method of claim ~~3~~4, wherein the delay mechanism uses cyclical redundancy checking.

6. (Original) The method of claim 5, wherein responding to the request comprises:

sending a response from the secondary component to the primary component.

7. (Original) The method of claim 1, wherein the arbitration logic is a simultaneous multiple primary component switching fabric.

8. (Original) The method of claim 7, wherein a plurality of secondary components are coupled to a plurality of primary components through the simultaneous multiple primary component switching fabric.

9. (Original) The method of claim 8, wherein the plurality of secondary components generate pseudo-random delays for requests from the plurality of primary components.

10. (Original) The method of claim 9, wherein the plurality of secondary components pseudo-random delay responses to requests from the plurality of primary components.

11. (Original) The method of claim 1, wherein the pseudo-random delay is used to adjust the wait-state of the secondary component.

12. (Original) The method of claim 1, wherein the pseudo-random delay is used to adjust the latency of the secondary component.

13. (Currently Amended) A secondary component, comprising:

an interface coupled to an interconnection module, the interface configured to communicate with a primary component through the interconnection module; and

a delay mechanism configured to determine values operable to delay responses to requests received through the interconnection module, wherein the values are pseudo-randomly generated values, wherein the values include a first value used to adjust the wait-state of the secondary component and a second value used to adjust the latency of the secondary component, wherein the wait-state is time the primary component has to wait before the second component accepts requests and the latency is time the secondary component takes to respond to the request.

14. (Original) The secondary component of claim 13, wherein the delay mechanism is configured to adjust the wait-state if the request is either a write request or a read request.

15. (Canceled)

16. (Previously Presented) The secondary component of claim 13, wherein the delay mechanism is a linear feedback shift register.

17. (Previously Presented) The secondary component of claim 13, wherein the delay mechanism uses cyclical redundancy checking.

18. (Previously Presented) The secondary component of claim 13, wherein the delay mechanism is configured to initiate a counter to execute the time delay.

19. (Previously Presented) The secondary component of claim 13, wherein the delay mechanism is configured to adjust the latency associated with the secondary component.

20. (Previously Presented) The secondary component of claim 13, wherein the delay mechanism is configured to adjust the wait-state associated with the secondary component.

21. (Currently Amended) A programmable chip, comprising:

a plurality of primary components, wherein the plurality of primary components are master components on the programmable chip;

a plurality of secondary components operable to receive requests from the plurality of primary components, wherein the plurality of secondary components are slave components on the programmable chip; and

arbitration logic coupling the plurality of primary components to the plurality of secondary components, the arbitration logic operable to arbitrate primary component access requests for secondary components;

wherein the plurality of secondary components are configured to determine delay values for adjusting response times to requests received through arbitration logic, wherein the values are pseudo-randomly generated values, wherein the values include a first value used to adjust the wait-state of the secondary component and a second value used to adjust the latency of the secondary component, wherein the wait-state is time the primary component has to wait before the second component accepts requests and the latency is time the secondary component takes to respond to the request.

22. (Original) The programmable chip of claim 21, wherein the plurality of primary and secondary components include processor and memory components.

23. (Original) The programmable chip of claim 21, wherein the plurality of secondary components are configured to adjust latency characteristics associated with response times.

24. (Original) The programmable chip of claim 21, wherein the plurality of secondary components are configured to adjust wait-state characteristics associated with response times.

25. (Original) The programmable chip of claim 21, wherein delay values are determined using a linear feedback shift register.

26. (Original) The programmable chip of claim 21, wherein delay values are determined using cyclical redundancy checking.

27. (Original) The programmable chip of claim 21, wherein the arbitration logic is operable to provide access to secondary components for multiple primary components simultaneously.

28. (Currently Amended) An apparatus for testing arbitration logic associated with a programmable chip system, the apparatus comprising:

means for receiving a request at a secondary component coupled to a primary component through arbitration logic, the request characteristic of a primary component request;

means for determining a pseudo-random delay at the secondary component prior to responding to the request; and

means for sending a response from the secondary component after the pseudo-random delay, the response corresponding to the request to test arbitration logic or bus-mastering logic associated with the digital logic device.~~pseudo-randomly delaying a response to the request.~~

29. (Currently Amended) The apparatus of claim 28, wherein the pseudo-random delay is used to adjust the wait-state of the secondary component, wherein the wait-state is an amount of time the primary component has to wait before the secondary component accepts the request.~~pseudo-randomly delaying comprises: means for adjusting the wait-state and/or latency.~~

30. (Original) The apparatus of claim 28, further comprising:

means for sending the delayed response from the secondary component to the primary component.